Short Papers

A New Simultaneous Noise and Input Power Matching Technique for Monolithic LNA's Using Cascode Feedback

Beom Kyu Ko and Kwyro Lee

***Abstract*— In this paper, a new simultaneous impedance-matching technique of $\Gamma_{\rm opt}$ (optimum noise-match source reflection coefficient) and $G_{\rm max}$ (maximum available power gain-match (MAPG) source reflection coefficient) using cascode feedback (CF) is proposed. A 1.57-GHz single-stage monolithic-microwave integrated-circuit (MMIC) low-noise amplifier (LNA) designed with this technique has been fabricated using GaAs MESFET technology in order to verify the feasibility of this scheme. The measured response agrees well with the simulated performance. Extensive computer simulation shows that when silicon npn bipolar junction transistor (BJT) is used, this scheme enables us to make both $\Gamma_{\rm opt}$ and $G_{\rm max}$ points near to 50 Ω, in addition to the simultaneous noise and input power matching. In addition, it has all the advantages of negative feedback such as stability, wider bandwidth, and insensitivity against parameter variation.**

***Index Terms*—Cascode, feedback, LNA, noise.**

I. Introduction

The low-noise amplifier (LNA) is one of the most important building blocks in the front end of a telecommunication system. It determines the noise figure and input voltage standing-wave ratio (VSWR) of the overall system because the first block signal fed from the antenna which it meets is the LNA. Thus, in order to improve the noise figure and input VSWR of the overall system, an LNA is required to have simultaneous low noise figure, high gain, and low-input VSWR.

When designing LNA's with a common-source single-gate FET (CSSG FET), it is well known that the noise matching for achieving the $NF_{\rm min}$ (minimum noise figure) has resulted in high input VSWR. This is because the $\Gamma_{\rm opt}$ (optimum noise-match source reflection coefficient) is usually very different from the $G_{\rm max}$ (maximum available power gain-match (MAPG) source reflection coefficient). So, some tradeoffs between noise figure, gain, and input VSWR are needed [1].

If, however, we can make $\Gamma_{\rm opt}$ and $G_{\rm max}$ coincident, $NF_{\rm min}$ (maximum power gain) and low VSWR can be simultaneously achieved. To achieve this aim, research have been done [1]–[4]. This paper proposes that the noise and the gain, and the input/output matching can be simultaneously achieved with good stability and wide bandwidth by combining the inherent advantages of the cascode and resistive-shunt feedback. This technique is more suitable for monolithic form than for hybrid because the device impedance level can be chosen at will by changing the gate size, thus the high-quality feedback resistance is easily available.

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The basic theory for this matching phenomenon is explained in Section II, with comparison to other LNA topologies described in Section III. The experimental result and conclusion are given in Sections IV and V, respectively.

II. Basic Theory

The basic schematic diagram of cascode-feedback LNA (CFLNA) consisting of cascoded MESFET's, resistive shunt feedback, and input/output matching networks is shown in Fig. 1, and uses several advantages of cascode and shunt feedback. Firstly, cascode-connected FET's provide much higher gain than CSSG FET's. Secondly, input and output matching can be done almost independently owing to much smaller S_{12}, which makes input/output tuning easier. Thirdly, shunt feedback gives much better stability. Finally, and most importantly, the simultaneous matching of $\Gamma_{\rm opt}$ and $G_{\rm max}$ can be achieved by judiciously choosing the value of the feedback resistance. Fig. 2 shows the impedance/admittance map of $\Gamma_{\rm opt}$, $G_{\rm max}$, and S_{11} of the CFLNA as a function of the feedback resistance at 4.5 GHz. The active device is 0.5 μm $\times$ 300 μm (75 μm $\times$ 4 fingers) GaAs MESFET from Samsung microwave semiconductor (SMS) foundry. The cutoff frequency f_T of this device is about 24 GHz. EEsof's Libra was used for simulation and circuit design throughout this paper. The characteristic impedance Z_0 is assumed to be 50 Ω unless stated otherwise.

It is very interesting to note that even in the case of very large feedback resistance, which is more than 20 times ($>$1000 Ω), the characteristic impedance $G_{\rm max}$ changes significantly, while $\Gamma_{\rm opt}$ and S_{11} remains almost unchanged as the value of feedback resistance varies. As the feedback resistance decreases (or feedback quantity increases), $G_{\rm max}$ moves closer to $\Gamma_{\rm opt}$ and finally coincides with it. That is, only the susceptance part of $G_{\rm max}$ changes considerably with decrease of the feedback resistance, while the conductance part moves along the constant conductance circle. This means that the simultaneous noise and input power matching is possible without added noise from the feedback resistance because of its large value. This is the key idea of this paper. In case of the feedback resistance that is less than about 1000 Ω, the moving of $G_{\rm max}$ is similar to those of $\Gamma_{\rm opt}$ and S_{11}^*. This, however, is not of much practical use because the gain becomes too small and the noise generated from the relatively small feedback resistance increases the $NF_{\rm min}$ of CFLNA considerably.

This is quite an unique and remarkable characteristic that the CF has. The resistive-shunt feedback circuit using CSSG FET does not have this property. Our theoretical analysis for CFLNA shows that constant conductance region of $G_{\rm max}$ occurs when $B = f_T/f$ is around 5 [6]. In the case of $B < 5$, the input conductance increases as the feedback resistance decreases. In the case of $B > 5$, the input conductance decreases to a certain point and starts to increase again as the feedback resistance decreases, as shown in Fig. 3. The simultaneous noise and input power matching is always possible with the proper choices of the device dimension and the feedback resistance.

III. Performance Comparison

Based on the following viewpoints such as gain, noise figure and/or noise measure, input VSWR with input noise-matched and

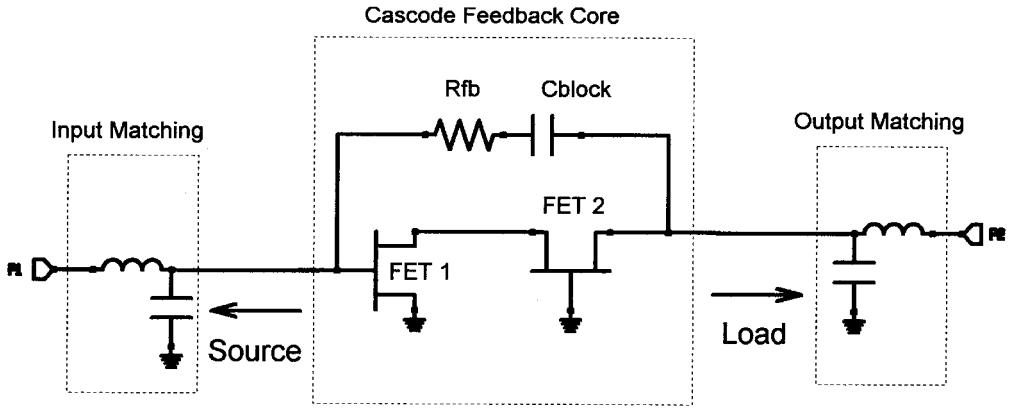

Fig. 1. Schematic diagram of the CF LNA with input/output matching network.

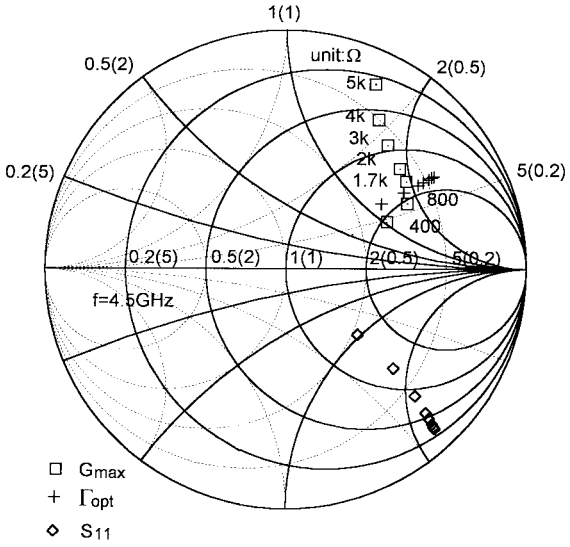

Fig. 2. Simulated impedance/admittance mapping of $\Gamma_{\rm opt}, G_{\rm max}$, and S_{11} of the CF versus the feedback resistance at 4.5 GHz $(f_T/f \cong 5)$ (solid line: impedance chart, dotted line: admittance chart). The device is 0.5 μm $\times$ 300 μm GaAs MESFET with 24 GHz of f_T. The values of the feedback resistance are chosen at 400, 800, 1.7000, 2000, 3000, 4000, and 5000 Ω, respectively. Note that as the feedback resistance decreases from 5000 Ω to 400 Ω, both $\Gamma_{\rm opt}$ and S_{11} points move toward the center of the Smith chart, but the $G_{\rm max}$ point changes quite dramatically from S_{11}^* and moves toward $\Gamma_{\rm opt}$.

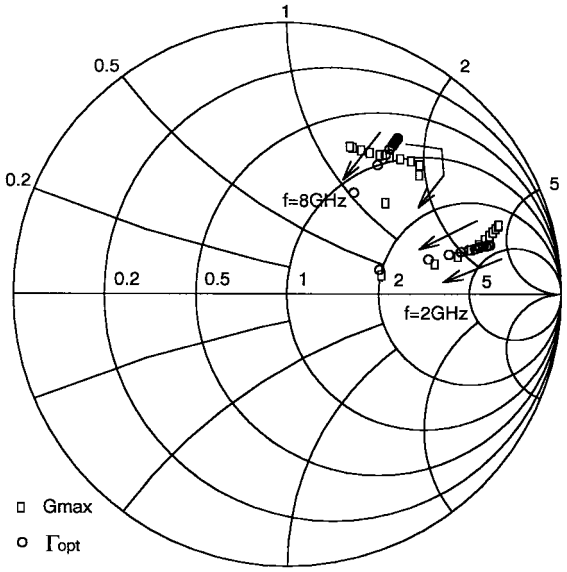

Fig. 3. Simulated impedance mapping of $\Gamma_{\rm opt}$ and $G_{\rm max}$ of the CF versus the feedback resistance at 2 GHz $(f_T/f = 12)$ and 8 GHz $(f_T/f = 3)$. The device is 0.5 μm $\times$ 300 μm GaAs MESFET with 24 GHz of f_T. The values of the feedback resistance are from 3.2 kΩ to 200 Ω with a 300-Ω step with the arrow direction.

output gain-matched, and stability, we compare this scheme with other conventional ones. The simulation results for the stability factor (K) [5], the MAG [5], the $NF_{\rm min}$, the normalized noise resistance (R_n), the minimum noise measure $(M_{\rm min})$ [1], and the input VSWR with the input noise-matched and the output gain-matched are given in Table I. In order for the MAG to be meaningful, the amplifier should be unconditionally stable, which means that the K should be larger than 1 and the B_1 should be larger than 0 [5]. In Table I, we omitted B_1 because the B_1 values of all the schemes which have $K > 1$ are larger than 0. When K is smaller than 1, the MAG means the maximum stable gain [5]. The used active devices are 0.5 μm $\times$ 300 μm GaAs MESFET (unit gate fingerwidth is 75 μm) and silicon npn bipolar junction transistor (BJT) with emitter area 20 μm $\times$ 6 μm from 0.8 μm BiCMOS process. The cutoff frequency f_T is about 24 GHz for the MESFET and 10 GHz for the BJT.

When the GaAs MESFET is used, the $M_{\rm min}$ of the CF with 5000 Ω feedback resistance is slightly larger than that of the CS and is much better than that of the CS with stabilization resistor at the load (CSRL) at the drain node and is comparable to that of the CS with series L inductor (CSSL) at the source node with an input VSWR of two as shown in Table I (see the parenthesis of CSSL). Also, note that the gain of the CF is much larger than that of other schemes without much sacrifice of $M_{\rm min}$ performance. This means that the number of LNA stages required to meet gain specification can be reduced with the CF scheme, which saves the dc-power dissipation while maintaining the comparable noise-measure performance. In addition, it has all the advantages of negative feedback such as stability, wider bandwidth, and insensitivity against parameter variation. The slight increase of $NF_{\rm min}$ of the CF is due to the added noise from the CG FET and the feedback resistance. In order to reduce the added noise, we have to make the gain of CS FET and the feedback resistance larger. Thus, this scheme becomes more suitable when n-p-n BJT is used as an active device because of the large transconductance. When

TABLE I
SIMULATED PERFORMANCE COMPARISON OF THE PROPOSED MATCHING TECHNIQUES WITH OTHER CONVENTIONAL ONES USING 0.5 μm × 300 μm GaAs MESFET (UNIT GATEWIDTH IS 75 μm) AT 2 GHz ($f_T/f = 12$) AND SILICON npn BJT WITH EMITTER AREA 20 μm × 6 μm FROM 0.8 μm BiCMOS PROCESS AT 1 GHz ($f_T/f = 10$)

Topologies	K	MAG (dB)	NFmin (dB)	Rn	Mmin	Input VSWR*(2)
CS (Common-Source)	0.133	17.3*(1)	0.57	0.850	0.144	--
CSRL (10Ω)	1.048	16.0	1.31	2.855	0.420	23.20
CSSL (4nH)	1.004	12.6 (12.1)	0.54 (0.79)	0.686	0.144 **(0.213)**	3.35 (2)
cascode	0.099	26.7*(1)	0.63	0.868	--	--
cascode feedback (2kΩ)	1.077	15.8	1.48	0.912	0.417	1.31
cascode feedback (5kΩ)	1.066	19.9	1.01	0.885	**0.266**	2
CE (Common-Emitter)	0.408	18.9*(1)	2.55	0.500	0.817	--
CERL (60Ω)	1.001	18.7	2.61	0.512	0.864	11.80
CESL (1.3nH)	1.003	15.7	2.51	0.445	0.817	4.10
cascode	-1.351	35.9*(1)	2.63	0.505	--	--
cascode feedback (R_{fb}=4kΩ & R_L=1.7kΩ)	1.107	27.2	2.72	0.506	**0.873**	1.24

*(1) Maximum stable gain (=10log|S_{21}/S_{12}|)

*(2) Input VSWR with the input noise-matched and the output gain-matched.

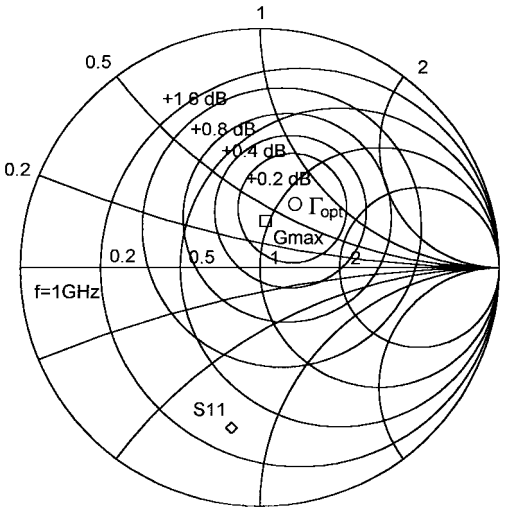

Fig. 4. Simulated constant noise-figure circles and $G_{\max}$ of the CF for 4000 Ω feedback resistor and 1.7000 Ω load resistor at 1 GHz. The device is an npn BJT with emitter area 20 μm × 6 μm from an 0.8-μm BiCMOS process.

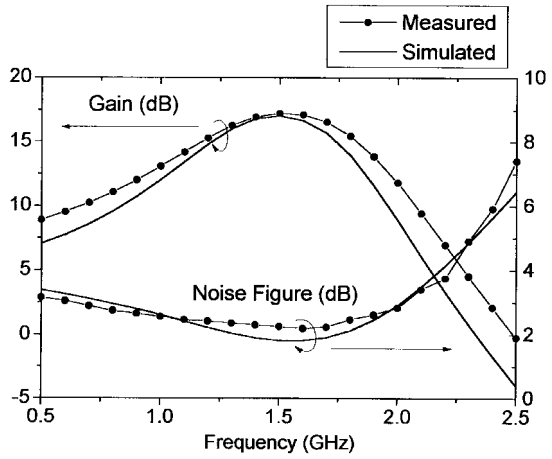

Fig. 5. Plot of measured versus simulated performance of the noise figure and the gain (S_{21}) of the fabricated CFLNA.

npn BJT is used, the $M_{\min}$ performance of CF is almost the same as that of the common-emitter (CE), as shown in Table I. This is due to the large transconductance of BJT and larger feedback resistance needed for matching. In addition, both $\Gamma_{\rm opt}$ and $G_{\max}$ points are very close to the 50-Ω point as well as the simultaneous noise and input power matching, as shown in Fig. 4. Thus, the CF scheme is very useful for LNA design using the npn BJT device at L-band.

IV. TEST RESULT

In order to see the feasibility of our approach, a 1.57-GHz single-stage monolithic LNA for a Global Positioning System (GPS) receiver application has been designed and fabricated with GEC Marconi 0.5-μm GaAs MESFET technology. The measured versus simulated performances of the noise figure, the gain, and the input/output return loss are shown in Figs. 5–7. It has demonstrated 2-dB noise figure with 17-dB gain and input/output return loss greater than 14–18 dB. The measured response agrees well with the simulated performance, which experimentally verifies our approach.

V. CONCLUSION

A new simultaneous impedance-matching technique of $\Gamma_{\rm opt}$ and $G_{\max}$ in the design of monolithic LNA's using cascode and resistive-shunt feedback has been developed. In order to check the feasibility of our approach, a 1.57-GHz single-stage monolithic microwave

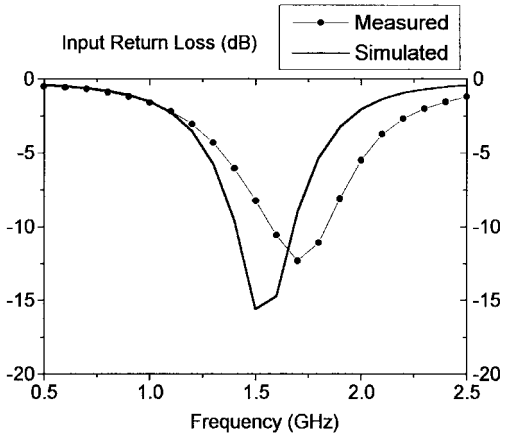

Fig. 6. Plot of measured versus simulated performance of the input return loss (S_{11}) of the fabricated CFLNA.

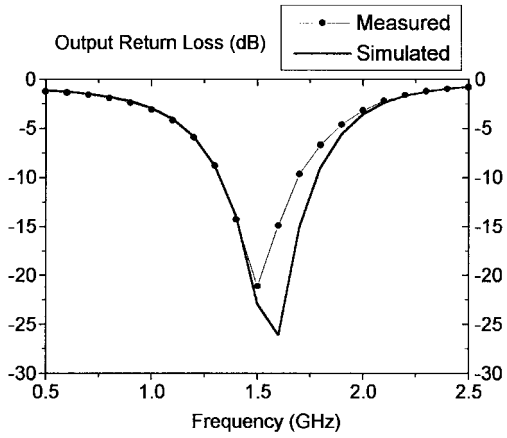

Fig. 7. Plot of measured versus simulated performance of the input return loss (S_{22}) of the fabricated CFLNA.

integrated circuit (MMIC) LNA has been fabricated. The measured response agrees well with the simulated performance. Extensive computer simulation shows that when silicon n-p-n BJT is used, this scheme enables us to make both $\Gamma_{\rm opt}$ and $G_{\rm max}$ points near to 50 Ω, in addition to the simultaneous noise and input power matching.

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A Large-Signal Characterization of an HEMT Using a Multilayered Neural Network

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***Abstract*—We propose an approach to describe the large-signal behavior of a high electron-mobility transistor (HEMT) by using a multilayered neural network. To conveniently implement this in standard circuit simulators, we extracted the HEMT's bias-dependent behavior in terms of conventional small-signal equivalent-circuit elements. We successfully represented seven intrinsic elements with a five-layered neural network (composed of 28 neurons) whose inputs are the gate-to-source bias $(V_{\rm gs})$ and drain-to-source bias $(V_{\rm ds})$. A "well-trained" neural network shows excellent accuracy and generates good extrapolations.**

***Index Terms*—HEMT, large-signal model, neural network.**

I. INTRODUCTION

A large-signal model for an active device, such as a high electron-mobility transistor (HEMT), is an essential tool for accurately designing high-frequency components. Several good models based on closed-form equations [1], [2] and look-up tables [3] have been proposed. Recently, a third approach using a neural network has been reported [4]. The neural-network model is an intermediate approach between the conventional ones, and accurately models a comparatively small database.

However, this reported neural-network model adopts a three-layered configuration which requires numerous neurons.

In this paper, we propose a different multilayered neural-network approach to describe the large-signal behavior of HEMT's. To conveniently implement it on a standard harmonic-balance simulator (such as the HP-MDS), we characterized large-signal behavior with a conventional small-signal equivalent-circuit analysis [5]. The bias-dependent intrinsic elements ($C_{\rm gs}$, R_i, C_{gd}, g_m, τ, $g_{\rm ds}$, and $C_{\rm ds}$) are then described by a neural network whose inputs are $V_{\rm gs}$ and $V_{\rm ds}$. We supplied normalized data for the neural network to obtain a learning convergence and stable extrapolations.

By experimenting, we found that a five-layered network configuration (consisting of only 28 neurons) adequately represents seven intrinsic elements simultaneously. We used a batch-mode back-propagation algorithm [6] and adopted this neural network to several similar devices. The well-trained network displayed excellent accuracy.

II. MULTILAYERED NEURAL NETWORK

Fig. 1 shows a standard multilayered (the number of layers is M) neural network. In this figure, each circle is a neuron, and the boxes enclosing several neurons are the layers. The kth layer includes $(N_k + 1)$ neurons. At the far left is the *input* layer, and at the far right is the *output* layer. The input and output of the ith neuron in

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